LYL MERCEDES CIGANDA BRASCA
Dr.

lmciganda@gmail.com
Manuel Otero 6354, CP. 11 500, Montevideo, Uruguay
0059899564795

SNI
Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información
Categorización actual: Iniciación (Asociado)

Fecha de publicación: 18/04/2019
Última actualización: 18/12/2015

Datos Generales

INSTITUCIÓN PRINCIPAL

Universidad de la República/ Facultad de Ingeniería - UDeLaR / Instituto de Ingeniería Eléctrica / Uruguay

DIRECCIÓN INSTITUCIONAL

Institución: Universidad de la República / Facultad de Ingeniería - UDeLaR / Sector Educación Superior/Público
Dirección: Julio Herrera y Reissig 565 / 11300 / Montevideo , Montevideo , Uruguay
Teléfono: (00598) 27110974 / 123
Correo electrónico/Sitio Web: lciganda@fing.edu.uy

Formación

Formación académica

CONCLUIDA

DOCTORADO

Computer and Control Engineering (2010 - 2013)

Politecnico di Torino , Italia
Título de la disertación/tesis/defensa: New Techniques for Reliability Characterization of Electronic Circuits
Tutor/es: Paolo Bernardi
Obtención del título: 2013
Sitio web de la disertación/tesis/defensa: http://porto.polito.it/id/eprint/2507391
Financiación:
Politecnico di Torino , Italia
Palabras Clave: reliability characterization integrated circuit testingsoftware-based self-test microprocessor digital logic design
Areas de conocimiento:
Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / Testing de circuitos electrònicos digitales/mixed signal

GRADO

Ingeniería Eléctrica (1998 - 2004)

Universidad de la República - Facultad de Ingeniería - UDeLaR , Uruguay
Título de la disertación/tesis/defensa: FitoInc. Un incubador para plantas.
Tutor/es: Enrique Ferreira
Obtención del título: 2004
Areas de conocimiento:
Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Sistemas de Automatización y Control / Control de temperatura

Idiomas

Español

Entiende muy bien / Habla muy bien / Lee muy bien / Escribe muy bien

Inglés

Entiende muy bien / Habla muy bien / Lee muy bien / Escribe muy bien

Italiano

Entiende muy bien / Habla muy bien / Lee muy bien / Escribe bien

Francés

Entiende regular / Habla regular / Lee regular / Escribe regular

Areas de actuación

INGENIERÍA Y TECNOLOGÍA

Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información /Hardware y Arquitectura de Computadoras

INGENIERÍA Y TECNOLOGÍA

Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información /Telecomunicaciones

INGENIERÍA Y TECNOLOGÍA

Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información /Ingeniería Eléctrica y Electrónica /Testing de circuitos electrònicos digitales

INGENIERÍA Y TECNOLOGÍA

Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información /Ingeniería Eléctrica y Electrónica /Education

INGENIERÍA Y TECNOLOGÍA

Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información /Ingeniería Eléctrica y Electrónica /Microprocessor Testing

INGENIERÍA Y TECNOLOGÍA

Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información /Ingeniería Eléctrica y Electrónica /diseño de circuitos digitales

Actuación profesional

SECTOR EDUCACIÓN SUPERIOR/PÚBLICO - UNIVERSIDAD DE LA REPÚBLICA - URUGUAY

Facultad de Ingeniería - UDeLaR

VÍNCULOS CON LA INSTITUCIÓN

Funcionario/Empleado (12/2008 - a la fecha) Trabajo relevante

6869 ,6 horas semanales
Desde 01-2010 hasta 02/2015 en licencia sin goce de sueldo para realizar estudios de postgrado en el exterior.
Escalafón: Docente
Grado: Grado 2
Cargo: Efectivo

Funcionario/Empleado (04/2004 - 12/2008)

,20 horas semanales
Escalafón: Docente
Grado: Grado 1
Cargo: Interino

SECTOR EMPRESAS/PÚBLICO - EMPRESA PÚBLICA - URUGUAY

Administración Nacional de Telecomunicaciones

VÍNCULOS CON LA INSTITUCIÓN

Funcionario/Empleado (03/2015 - a la fecha) Trabajo relevante

Ingeniero Eléctrico Nivel B ,40 horas semanales

Funcionario/Empleado (05/2005 - 01/2010)

Ingeniro Civil/Electrico ,40 horas semanales

Becario (11/2001 - 05/2005)

Becario Estudiante de Ingenieria ,30 horas semanales

SECTOR EXTRANJERO/INTERNACIONAL/OTROS - ITALIA

Politecnico di Torino

VÍNCULOS CON LA INSTITUCIÓN

Funcionario/Empleado (07/2013 - 12/2014) Trabajo relevante

Post Doc Research Fellow ,50 horas semanales / Dedicación total

Funcionario/Empleado (01/2013 - 06/2013)

Research Fellow ,50 horas semanales / Dedicación total

Becario (01/2010 - 12/2012)

PhD Student ,50 horas semanales / Dedicación total

ACTIVIDADES

DOCENCIA

Computer and Control Engineering (03/2010 - 12/2014)

Grado
Asistente
Asignaturas:
Informática (Lenguaje C), 3 horas, Práctico

SECTOR EXTRANJERO/INTERNACIONAL/OTROS - FRANCIA

Institut National Polytechnique de Grenoble

VÍNCULOS CON LA INSTITUCIÓN

Colaborador (09/2012 - 01/2013)

Visitante ,50 horas semanales / Dedicación total
The dynamic performances of an ADC reflect the noise and the distortion introduced by the ADC in its signal path. They are measured by injecting a single-tone sine-wave signal at the input of the ADC and computing a fast Fourier transform (FFT) of the output. In the context of a Built-In Self-Test technique that aims to compute the dynamic performances on-chip, it is required to replace the computationally intensive FFT algorithm with an alternative algorithm that can be implemented efficiently. Two algorithms are known for computing the signal to noise and distortion ratio (SNDR) dynamic performance: the sine wave fitting and the CORDIC algorithms. The proposed research work aims to determine first which of the two algorithms is more suitable given the constraints of a BIST implementation (i.e. accuracy, robustness, silicon overhead, etc.). For this purpose, a theoretical study is required for determining their accuracy. Then, the implementation of one of the algorithms in digital circuitry (VHDL, RTL, layout, verification, etc.) will be carried out. Finally, a solution for computing the total harmonic distortion (THD) and signal to noise ratio (SNR) dynamic performances through these algorithms will be studied.

CARGA HORARIA

Carga horaria de docencia: 4 horas
Carga horaria de investigación: 2 horas
Carga horaria de formación RRHH: 2 horas
Carga horaria de extensión: Sin horas
Carga horaria de gestión: 38 horas

Producción científica/tecnológica

My work falls in the low cost testing domain. Strategies for new and/or improved SBST, DfT and ATE mechanisms are proposed, implemented and evaluated. The strategies deal mainly with memories, processor and mixed-signal devices (analogue-to-digital converters is our target device) embedded in Systems-on-a-Chip, where standard communication protocols and wrappers are used to communicate with the device under test.
Integrated electronic systems are increasingly used in an wide number of applications and environments, ranging from critical missions to low cost consumer products. However, there are many difficult challenges associated with continued cost reduction, size reduction, improved performance and improved power efficiency.
One of these challenges is the reliability of these electronic systems. Manufacturing processes, intrinsic aging phenomena of components and environmental stress may cause internal defects and damages during the lifetime of a system, possibly causing misbehaviours or failures. In order to guarantee product quality and consumer satisfaction, it is necessary not only to discover faults as soon as possible in the manufacturing process, but also to continuously check for their absence throughout a product lifetime.
With testers being expensive pieces of equipment and the cost of transistors continuously decreasing, it makes sense to use some of these low-cost transistors to replace the costly test tools, whenever possible.
The first low cost approach we can think about is using the devices themselves to implement their own test. This is the underlying motivation of functional Software-Based Self-Test (SBST): a fast, powerful microprocessor, which has lots of resources, could certainty help in its testing procedure. Having the advantages of enabling at-speed testing, zero area overhead and actually testing the devices operation, this approach also has some drawbacks. Even if SBST is essentially suitable for online testing (and sometimes it is the only possible approach), it requires some dedicated system memory for the functional testing data, which can reach very big sizes. Also some faults happen to be functionally untestable.
A second approach to low cost testing is design for test (DfT). Add some extra (cheap) area on-chip specifically in charge of performing tests. The DfT path started long ago, but it is still a key element in 2013 International Technology Roadmap for Semiconductors test roadmap. Logic and Memory Built-In Self Test schemas are usual practises. Analogue DfT is also an interesting strategy, especially when the analogue or mixed-signal device is integrated in a wider digital system like a SoC.
Finally, there are some fields where the use of external (and generally expensive) testers is mandatory. Diagnosis is a case in which an Automatic Test Equipment (ATE) is needed to store the huge amount of retrieved data and to drive the cyclic characteristic of the diagnosis procedure. In particular, memories diagnosis. Another interesting and blooming field is that of the mixed energy-domain devices as Micro Electro Mechanical Systems (MEMS). MEMS require unique testing apparatus applying both electrical and physical stimuli: movement, pressure, magnetic fields.

Producción bibliográfica

ARTÍCULOS PUBLICADOS

ARBITRADOS

MIHST: A Hardware Technique for Embedded Microprocessor Functional On-line Self-Test (Completo, 2013) Trabajo relevante

L. M. CIGANDA
IEEE Transactions on Computers, v.: PP 99 , 2013
Palabras clave: Built-in self-test Microprocessors Online test
Areas de conocimiento:
Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / Testing de circuitos electrònicos digitales/mixed signal
Medio de divulgación: Internet
ISSN: 00189340
DOI: 10.1109/TC.2013.165
http://ieeexplore.ieee.org/xpl/articleDetails.jsp?tp=&arnumber=6579592&queryText%3Dciganda
Abstract Testing processor cores embedded in Systems-on-Chip (SoCs) is a major concern for industry nowadays. In this paper, we describe a novel solution which merges the SBST and BIST principles. The technique we propose forces the processor to execute a compact SBST-like test sequence by using a hardware module called MIcroprocessor Hardware Self-Test (MIHST) unit, which is intended to be connected to the system bus like a normal memory core, requesting no

modification of the processor core internal structure. The benefit of using the MIHST approach is manifold: while guaranteeing the same or higher defect coverage of the traditional SBST approach, it reduces the time for test execution, better preserves the processor core Intellectual Property (IP), does not require the system memory to store the test program nor the test data, and can be easily adopted for non-concurrent on-line testing, since it minimizes the required system resources. The feasibility and effectiveness of the approach were evaluated on a couple of pipelined processors.
Scopus WEB OF SCIENCE™

An Adaptive Low-Cost Tester Architecture Supporting Embedded Memory Volume Diagnosis (Completo, 2012) Trabajo relevante

L. M. CIGANDA
IEEE Transactions on Instrumentation and Measurement, v.: 61 4 , p.:1002 - 1018, 2012
Palabras clave: Built-in self-test embedded systems Random access memory IEEE 1500 wrappers adaptive low cost tester architecture fault diagnosis
Areas de conocimiento:
Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / Testing de circuitos electrònicos digitales/mixed signal
Medio de divulgación: Papel
ISSN: 00189456
DOI: 10.1109/TIM.2011.2179822
http://ieeexplore.ieee.org/xpls/icp.jsp?arnumber=6146456
Abstract This paper describes the working principle and an implementation of a low-cost tester architecture supporting volume test and diagnosis of built-in self-test (BIST)-assisted embedded memory cores. The described tester architecture autonomously executes a diagnosis-oriented test program, adapting the stimuli at run-time, based on the collected test results. In order to effectively allow the tester architecture to interact with the devices under test with an acceptable time overhead, the approach exploits a special hardware module to manage the diagnostic process. Embedded static RAMs equipped with diagnostic BISTs and IEEE 1500 wrappers were selected as case study; experimental results show the feasibility of the approach when having a field-programmable gate array available on the tester and its effectiveness in terms of diagnosis time and required tester memory with respect to traditional testers executing diagnosis procedures by means of software running on the host computer.
Scopus WEB OF SCIENCE™

A Parallel Tester Architecture for Accelerometer and Gyroscope MEMS Calibration and Test (Completo, 2011) Trabajo relevante

L. M. CIGANDA
Journal of Electronic Testing: Theory and Applications, v.: 27 3 , p.:389 - 402, 2011
Palabras clave: MEMS testing MEMS calibration Accelerometer Gyroscope Automatic Test System
Areas de conocimiento:
Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / Testing de circuitos electrònicos digitales/mixed signal
Medio de divulgación: Papel
Lugar de publicación: Springer US
ISSN: 09238174
DOI: 10.1007/s10836-011-5210-2
http://link.springer.com/article/10.1007%2Fs10836-011-5210-2/fulltext.html
Abstract This paper describes a tester architecture for Accelerometer and Gyroscope Micro-ElectroMechanical System (MEMS) devices test and calibration, allowing increased parallelism rate and process accuracy. The proposed tester architecture tackles some critical issues related to MEMS testing, such as mitigating mechanical concerns that potentially impact on the equipment Mean Time Between Maintenance and guaranteeing a sufficient number of measurements in the time unit. The proposed strategy consists in an innovative and low cost tester resource partitioning that overcomes current limitations to multisite Accelerometer and Gyroscope MEMS testing. A tester prototype was implemented exploiting FPGAs; feasibility and effectiveness of the proposed methodology was demonstrated on commercial accelerometer and gyroscope MEMS devices. Topics Computer-Aided Engineering (CAD, CAE) and Design Electrical Engineering Circuits and Systems Industry Sectors IT & Software Electronics Engineering Aerospace Telecommunications Automotive
Scopus WEB OF SCIENCE™

LIBROS

Exercising Creativity 2012 (Participación , 2013)

Baklanova Elena , L. M. CIGANDA , JING TIAN G. , MIRZAEI P. , SANABRIA J. , WANG XUEYUN J.
Número de volúmenes: 1
Edición: 1,
Editorial: Editorial Universitat Politécnica de Valéncia, Valéncia
Palabras clave: creativity engineering
Areas de conocimiento:
Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / Elecrtonica aplicada y comercializacion
Medio de divulgación: Papel
ISSN/ISBN: 9788490480489

Capítulos:
E-Heels
Organizadores: Daniel Collado-Ruiz, Hesamedin Ostad-Ahmad-Ghorabi
Página inicial 57, Página final 66

PUBLICACIÓN DE TRABAJOS PRESENTADOS EN EVENTOS

An effective approach to automatic functional processor test generation for small-delay faults (2014)

Completo
RIEFERT A. , L. M. CIGANDA , SAUER M. , BERNARDI P. , SONZA REORDA M. , BECKER B.

Evento: Internacional
Descripción: Design, Automation and Test in Europe Conference and Exhibition (DATE)
Ciudad: Dresden (Germany)
Año del evento: 2014
Pagina inicial: 1
Pagina final: 6
Publicación arbitrada
Editorial: IEEE - INST ELECTRICAL ELECTRONICS ENGINEERS INC
Palabras clave: automatic test pattern generation microprocessor chips functional processor test at-speed execution bounded model checking miniMIPS
Areas de conocimiento:
Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / Microprocessor Testing
Medio de divulgación: CD-Rom
DOI: 10.7873/DATE2014.140
Functional microprocessor test methods provide several advantages compared to DFT approaches, like reduced chip cost and at-speed execution. However, the automatic generation of functional test patterns is an open issue. In this work we present an approach for the automatic generation of functional microprocessor test sequences for small-delay faults based on Bounded Model Checking. We utilize an ATPG framework for small-delay faults in sequential, non-scan circuits and propose a method for constraining the input space for generating functional test sequences (i.e., test programs). We verify our approach by evaluating the miniMIPS microprocessor. In our experiments we were able to reach over 97 % fault efficiency. To the best of our knowledge, this is the first fully automated approach to functional microprocessor test for small-delay faults.

An efficient method for the test of embedded memory cores during the operational phase (2013)

Completo
BERNARDI P. , L. M. CIGANDA , SONZA REORDA M. , HAMDIOUI S.

Evento: Internacional
Descripción: 22nd Asian Test Symposium
Ciudad: Yilan (Taiwan)
Año del evento: 2013
Pagina inicial: 227
Pagina final: 232
ISSN/ISBN: 10817735
Publicación arbitrada
Editorial: IEEE Computer Society (USA)
Palabras clave: system-on-chip memory testing ad hoc module March tests safety critical application software BIST
Areas de conocimiento:
Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información /

Ingeniería Eléctrica y Electrónica / Memory Testing
Medio de divulgación: Papel
DOI: 10.1109/ATS.2013.50
System on Chip devices include an increasing number of embedded memory cores, whose test during the operational phase is often a strict requirement, especially for safety-critical applications. This paper proposes a new memory test method combining the characteristics of hardware and software solutions: the test is performed by the microcontroller/processor, while the code of the test instructions to be executed is generated on-the-fly by an ad hoc module, also in charge of checking the memory behavior. The solution is modular and does not require any modification either in the memory cores or in the processor. Moreover, it is well suited to be used for test during the operational phase. Experimental results, gathered by implementing some representative March elements and algorithms, show that the method guarantees higher defect coverage than software BIST and a test time comparable with that of traditional hardware BIST solutions with a reduced hardware cost.

Automatic Generation of On-Line Test Programs through a Cooperation Scheme (2012)

Completo
L. M. CIGANDA

Evento: Internacional
Descripción: International Workshop on Microprocessor Test and Verification (MTV)
Ciudad: Austin TX, USA
Año del evento: 2012
Anales/Proceedings:IEEE Proceedings of the 13th International Workshop on Microprocessor Test and Verification (MTV)
Pagina inicial: 13
Pagina final: 18
ISSN/ISBN: 9781467344418
Publicación arbitrada
Palabras clave: Group Evolution System on Chip pipelined processors software-based self-test on-line testing
Areas de conocimiento:
Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / Testing de circuitos electrònicos digitales/mixed signal
Medio de divulgación: Internet
Abstract Test programs for Software-based Self-Test (SBST) can be exploited during the mission phase of microprocessor-based systems to periodically assess hardware integrity. However, several additional constraints must be imposed due to the coexistence of test programs with the mission application. This paper proposes a method for the generation of SBST on-line test programs for embedded RISC processors, systems where the impact of on-line constraints is significant. The proposed strategy exploits an evolutionary optimizer that is able to create a complete test set of programs relying on a new cooperative scheme. Experimental results showed high fault coverage values on two different modules of a MIPS-like processor core. These two case studies demonstrate the effectiveness of the technique and the low human effort required for its implementation.

On-Line Software-Based Self-Test of the Address Calculation Unit in RISC Processors (2012)

Completo
BERNARDI P. , L. M. CIGANDA , DE CARVALHO M. , GROSSO M. , LAGOS-BENITES J. , SáNCHEZ E. , SONZA REORDA M. , BALLAN O.

Evento: Internacional
Descripción: 17th IEEE European Test Symposium (ETS)
Ciudad: Annecy (FR)
Año del evento: 2012
Pagina inicial: 1
Pagina final: 6
ISSN/ISBN: 9781467306966
Publicación arbitrada
Editorial: IEEE
Palabras clave: pipelined processors software-based self-test on-line testing microprocessor embedded RISC processor Testing
Areas de conocimiento:
Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / Microprocessor Testing

Medio de divulgación: Papel
DOI: 10.1109/ETS.2012.6233004
Software-based Self-Test (SBST) can be used during the mission phase of microprocessor-based systems to periodically assess the hardware integrity. However, several constraints are imposed to this approach, due to the coexistence of test programs with the mission application. This paper proposes a method for the generation of SBST programs to test on-line the Address Calculation Unit of embedded RISC processors, which is one of the most heavily impacted by the online constraints. The proposed strategy achieves high stuck-at fault coverage on both a MIPS-like processor and an industrial 32-bit pipelined processor; these two case studies show the effectiveness of the technique and the low effort.

A SBST strategy to test microprocessors' branch target buffer (2012)

Completo
BERNARDI P. , L. M. CIGANDA , GROSSO M. , SáNCHEZ E. , SONZA REORDA M.

Evento: Internacional
Descripción: IEEE 15th International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS)
Ciudad: Tallinn (Estonia)
Año del evento: 2012
Pagina inicial: 1
Pagina final: 6
ISSN/ISBN: 9781424497546
Publicación arbitrada
Editorial: IEEE
Palabras clave: software-based self-test microprocessor branch prediction branch target buffer pipelined microprocessor functional testing method
Areas de conocimiento:
Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / Microprocessor Testing
Medio de divulgación: Papel
DOI: 10.1109/DDECS.2012.6219079
A Branch Target Buffer (BTB) is a mechanism to support speculative execution in order to overcome the performance penalty caused by branch instructions in pipelined microprocessors. Being an intrinsically fault tolerant unit, it is hard to achieve a good fault coverage resorting to plain functional testing methods. In this paper we analyze the causes for low functional testability and propose some techniques able to effectively face these issues. In particular, we describe a strategy to perform SBST on fully associative BTB units. The unit's general structure is analyzed, a suitable test program is proposed and the strategy to observe the test responses is explained. Feasibility and effectiveness of the proposed approach are shown on a MIPS-like processor.

An Effective Methodology for On-line Testing of Embedded Microprocessors (2011) Trabajo relevante

Completo
BERNARDI P. , L. M. CIGANDA , SáNCHEZ E. , SONZA REORDA M.

Evento: Internacional
Descripción: IEEE 17th International on-line testing symposium (IOLTS)
Ciudad: Atene (GR)
Año del evento: 2011
Pagina inicial: 1
Pagina final: 6
ISSN/ISBN: 9781457710537
Publicación arbitrada
Palabras clave: Built-in self-test integrated circuit testing system-on-chip microprocessor On-line test
Areas de conocimiento:
Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / Microprocessor Testing
Medio de divulgación: Papel
DOI: 10.1109/IOLTS.2011.5994541
Testing embedded microprocessors at mission time is nowadays a requirement in many SoC applications. In this paper, we introduce a methodology where the detection of operational faults is performed while the normal operations are temporarily suspended, by means of an ad-hoc HW module connected to the address, data and control buses of the microprocessor. This module

behaves as a peripheral towards the microprocessor but is able to gain access to the bus over the system memory during the test. The proposed approach uses the microprocessor interrupt protocol to preserve the system state. Experimental results, gathered on a MIPS core, show the feasibility and effectiveness of the approach.

A tester architecture suitable for MEMS calibration and testing (2010)

Completo
L. M. CIGANDA , BERNARDI P. , SONZA REORDA M. , BARBIERI D. , STRAIOTTO M. , BONARIA L.

Evento: Internacional
Descripción: International Test Conference (ITC)
Ciudad: Austin, TX (USA)
Año del evento: 2010
ISSN/ISBN: 10893539/97814
Publicación arbitrada
Editorial: IEEE
Palabras clave: MEMS testing MEMS calibration micromechanical devices electrical stimuli tester architecture
Areas de conocimiento:
Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / MEMS Testing
Medio de divulgación: Papel
This poster outlines the working principle and an implementation of a tester architecture supporting MEMS calibration and testing; the tester works adaptively, providing electrical stimuli at run-time according to the collected results. The tester manages the calibration and testing process by means of a special hardware module, saving time and avoiding tester parallelism limitations due to massive wiring. Feasibility and effectiveness of the proposed method have been evaluated through simulations before being possibly introduced in commercial MEMS accelerometer testers.

Diseño de placas con lógica programable como experiencia educativa en cursos de grado. (2009)

Completo
FERNáNDEZ S. , BERGERET A. , L. M. CIGANDA , OLIVER J. P.

Evento: Internacional
Descripción: IX Jornadas de Computación Reconfigurable y Aplicaciones
Ciudad: Alcalá de Henares (ES)
Año del evento: 2009
Anales/Proceedings:Actas de las IX jornadas de computación reconfigurable y aplicaciones
Pagina inicial: 1
Pagina final: 10
ISSN/ISBN: 9788481388329
Publicación arbitrada
Editorial: Universidad de Alcalá
Areas de conocimiento:
Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / Enseñanza

An enhanced FPGA-based low-cost tester platform exploiting effective test data compression for SoCs (2009)

Completo
L. M. CIGANDA , ABATE F. , BERNARDI P. , BRUNO M. , SONZA REORDA M.

Evento: Internacional
Descripción: 12th International Symposium on Design and Diagnostics of Electronic Circuits & Systems
Ciudad: Liberec (CZ)
Año del evento: 2009
Pagina inicial: 1
Pagina final: 6
ISSN/ISBN: 9781424433414
Publicación arbitrada
Palabras clave: integrated circuit testing design for testability system-on-chip FPGA based tester test compression / decompression Automatic testing
Areas de conocimiento:

Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / Digital Circuits Testing
Medio de divulgación: Papel
Reducing the cost of test (in particular by reducing its duration and the cost of the required ATE) is a common goal which has largely been pursued in the past, mainly by introducing suitable on chip Design for Testability (DfT) circuitry. Today, the increasing popularity of sophisticated DfT architectures and the parallel emergence of new ATE families allow the identification of innovative solutions effectively facing that goal. In this paper we face the increasingly common situation of SoCs adopting the IEEE 1149.1 and 1500 standards for the test of the internal cores, and explore the idea of storing the test program on the tester in a compressed form, and decompressing it on-the-fly during test application. This paper proposes an improved version of an data compression/decompression technique which is well suited for reducing the size of test programs stored on the tester; this technique is particularly effective for very long sequential test vectors generated to test SoCs by means of low-cost test procedures; thus, the paper outlines the characteristics of an FPGA-based low-cost tester platform that takes advantage of the described compression schema. The effectiveness of the proposed methodology was demonstrated by practically testing some SoCs equipped with suitable DfT for supporting low-cost testing resorting to a low-cost tester implementing the proposed architecture and the compression/decompression technique.

Laboratory at Home: Actual Circuit Design and Testing Experiences in Massive Digital Design Courses (2006)

Completo
HAIM F. , FERNáNDEZ S. , RODRíGUEZ J , L. M. CIGANDA , ROLANDO, P. , OLIVER J. P.

Evento: Internacional
Descripción: 9th International Conference on Engineering Education
Ciudad: San Juan (PR)
Año del evento: 2006
Pagina inicial: 5
Pagina final: 9
Publicación arbitrada
Palabras clave: computer aided instruction distance learning electronic engineering education logic design hardware kits lab at home
Areas de conocimiento:
Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / Education
Medio de divulgación: Papel
An innovative laboratory methodology for thedigital design introductory course is presented. We replacethe traditional lab experiences, where students have tocome to school classrooms, with a lab at home concept.More than 65 kits with a programmable logic board aregiven to groups of students for the whole semester. Thus,students perform all the lab stages, including analyzing theproblems, designing a solution and testing the actualcircuit, at their homes. Then, they come to school to showtheir circuits to the professors. These evaluation instances,together with a final exam, are enough to adequatelyevaluate the students work, eliminating the need of a mid-term exam. This is the third edition of the course with thismethodology. A survey of opinion showed that theexperience was very successful among students. Moreover,it is very suitable for massive courses and easily scalable,providing actual hardware platforms for students at anaffordable cost for the institution.

Laboratorios en casa: Una Nueva Alternativa Para Cursos Masivos de Diseño Lógico Digital (2006)

Completo
OLIVER J. P. , FERNáNDEZ S. , HAIM F. , RODRíGUEZ J , L. M. CIGANDA , ROLANDO, P.

Evento: Internacional
Descripción: VII Congreso de Tecnologías Aplicadas a la Enseñanza de la Electrónica
Ciudad: Madrid (ES)
Año del evento: 2006
Pagina inicial: 1
Pagina final: 7
ISSN/ISBN: 9788468995908
Publicación arbitrada
Palabras clave: Enseñanza Diseño digital laboratorio@home
Areas de conocimiento:

Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / Enseñanza
Medio de divulgación: Papel

Evaluaciones

EVALUACIÓN DE PUBLICACIONES

COMITÉ EDITORIAL

Journal of Electronic Testing: Theory and Applications (2014 / 2014)

Cantidad: Menos de 5
Review of manuscript: "VHDL Modelling of Full Fault Detection Coverage Memory Tester"

Very Large Scale Integration of System-on-Chip (VLSI-SoC) (2014 / 2014)

Cantidad: Menos de 5

Formación de RRHH

TUTORÍAS CONCLUIDAS

POSGRADO

Implementation and Testing of a Parametric Branch Prediction Unit in Pipelined Processors (2012)

Tesis de maestria
Sector Extranjero/Internacional/Otros / Politecnico di Torino , Italia
Programa: Electronic Engineering
Nombre del orientado: FU Mengyang
Medio de divulgación: Papel
País/Idioma: Italia, Inglés
Palabras Clave: software-based self-test branch prediction branch target buffer Testing of processors
Areas de conocimiento:
Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / Microprocessor Testing
Branch instructions can possibly reduce the performance of pipelined processors by interrupting the steady instruction flow into the pipeline. In past decades, several strategies have been developed to solve this problem. Among them, Branch Target Buffer (BTB) is a method which uses a small associated memory to store the information of several executed branches. The prediction based on these information will significantly improve the performance of pipelined processors. However, this kind of prediction units brings difficulties on testing due to their deeply embedded architectures. This thesis proposes a design of a parametric branch prediction unit using a BTB with 2-bit predictor in pipelined processors. Then in order to test such prediction units, Software Based Self-Test (SBST) method is introduced. Adopting this method, suitable test strategies are proposed considering the structure of the BTB and the test programs for the prediction unit are developed and explained based on a processor core with MIPS architecture. This method used is effective and cost-economical on testing such prediction units. Moreover, both of the proposed design and testing approaches could be transplanted to other MIPS-like processors with a limited effort.

Otros datos relevantes

PRESENTACIONES EN EVENTOS

15th IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems (2012)

Simposio
A SBST strategy to test microprocessors' branch target buffer
Estonia
Tipo de participación: Expositor oral
Carga horaria: 24
Nombre de la institución promotora: IEEE

Palabras Clave: software-based self-test microprocessor branch target buffer functional testing method Branch prediction unit test program
Areas de conocimiento:
Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / Microprocessor Testing
A Branch Target Buffer (BTB) is a mechanism to support speculative execution in order to overcome the performance penalty caused by branch instructions in pipelined microprocessors. Being an intrinsically fault tolerant unit, it is hard to achieve a good fault coverage resorting to plain functional testing methods. In this paper we analyze the causes for low functional testability and propose some techniques able to effectively face these issues. In particular, we describe a strategy to perform SBST on fully associative BTB units. The unit's general structure is analyzed, a suitable test program is proposed and the strategy to observe the test responses is explained. Feasibility and effectiveness of the proposed approach are shown on a MIPS-like processor.

17th IEEE International On-Line Testing Symposium (2011)

Simposio
An Effective Methodology for On-line Testing of Embedded Microprocessors
Grecia
Tipo de participación: Expositor oral
Carga horaria: 24
Nombre de la institución promotora: IEEE
Palabras Clave: Built-in self-test system-on-chip microprocessor On-line test ad hoc hardware module
Areas de conocimiento:
Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / Microprocessor Testing
Testing embedded microprocessors at mission time is nowadays a requirement in many SoC applications. In this paper, we introduce a methodology where the detection of operational faults is performed while the normal operations are temporarily suspended, by means of an ad-hoc HW module connected to the address, data and control buses of the microprocessor. This module behaves as a peripheral towards the microprocessor but is able to gain access to the bus over the system memory during the test. The proposed approach uses the microprocessor interrupt protocol to preserve the system state. Experimental results, gathered on a MIPS core, show the feasibility and effectiveness of the approach.

International Test Conference (2010)

Congreso
A tester architecture suitable for MEMS calibration and testing
Estados Unidos
Tipo de participación: Poster
Carga horaria: 40
Nombre de la institución promotora: IEEE
Palabras Clave: MEMS testing MEMS calibration FPGA based tester test compression / decompression Automatic Test Equipment parallel testing
Areas de conocimiento:
Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería Eléctrica y Electrónica / MEMS Testing
This poster outlines the working principle and an implementation of a tester architecture supporting MEMS calibration and testing; the tester works adaptively, providing electrical stimuli at run-time according to the collected results. The tester manages the calibration and testing process by means of a special hardware module, saving time and avoiding tester parallelism limitations due to massive wiring. Feasibility and effectiveness of the proposed method have been evaluated through simulations before being possibly introduced in commercial MEMS accelerometer testers.

JURADO/INTEGRANTE DE COMISIONES EVALUADORAS DE TRABAJOS ACADÉMICOS

Commissioni per gli Esami di Laurea della Sessione del mese di novembre 2012, dei corsi di studio afferenti al Collegio di Ingegneria Informatica, del Cinema e Meccatronica. (2012)

Candidato: Cosenza,Domingo,Fu,Gullo,Pasturenzi,Rosato,Sandiano,Vasciave
Tipo Jurado: Tesis de Maestría
BERNARDI P. , SáNCHEZ E. , BENSO A. , DI CARLO S. , MORISIO M. , SQUILLERO G. , L. M. CIGANDA
Computer Engineering / Sector Extranjero/Internacional/Otros / Institución Extranjera / Politecnico di Torino / Italia

País: Italia
Idioma: Inglés
Areas de conocimiento:
Ingeniería y Tecnología / Ingeniería Eléctrica, Ingeniería Electrónica e Ingeniería de la Información / Ingeniería de Sistemas y Comunicaciones / Education
Comisión que evaluaba 7 trabajos de tesis de maestría de 8 autores, todos en el ámbito de la ingeniería informática.

Indicadores de producción

PRODUCCIÓN BIBLIOGRÁFICA	**15**
Artículos publicados en revistas científicas	3
Completo	3
Trabajos en eventos	11
Libros y Capítulos	1
Capítulos de libro publicado	1
EVALUACIONES	**2**
Evaluación de publicaciones	2
FORMACIÓN RRHH	**1**
Tutorías/Orientaciones/Supervisiones concluidas	1
Tesis de maestria	1